Muhammad Sarmad Sohail

+92 323 854 0201 | msarmadsohail@gmail.com | msarmadsohail | msarmadsohail | Portfolio

Education

National University of Sciences and Technology (NUST) *Islamabad, Pakistan*
Bachelor of Electrical Engineering *Sep. 2020 – Jun. 2024*

- **CGPA:** 3.70/4.00
- **Thesis:** Resource Allocation for MEC-Enabled CR-NOMA Networks using DRL | Paper | Demo | Poster
  Advised by Dr. Syed Ali Hassan
- **Key Courses:** Mobile Communication Systems, Machine Learning, Digital Signal Processing, Embedded System Design, Robotics, Digital System Design, Bitcoin & Cryptocurrencies, Probability & Statistics

Industry Experience

Adept Tech Solutions (ATS) *Sept. 2025 – Present*
Data Engineer *Pleasanton, California (Remote)*

- Develop backend microservices using **Python** and **FastAPI** to expose statistical analysis, preprocessing, and synthetic data generation capabilities for the ASCEND Synthetic Data Platform
- Maintain and extend production-grade modules for data profiling, feature engineering, anonymization, imputation, and synthetic data generation
- Orchestrate distributed **PySpark** workloads for ETL pipelines, ensuring scalable execution of synthetic data generation across large datasets

Xcelerium *Jan. 2025 – May. 2025*
Trainee Engineer - Analog & Mixed Signal IC Design *Islamabad, Pakistan*

- Designed a 100 MHz 7-bit SAR ADC in **TSMC 28nm** PDK using **Cadence Virtuoso**, integrating bootstrapped sampling switches, dynamic latch comparators, and a binary-weighted capacitive DAC
- Designed a high-speed 12-bit SAR ADC prototype in **GF 22nm FD-SOI** PDK using **Synopsys Custom Compiler**, implementing triple-tail comparators, non-overlapping clock generation, and custom SAR logic blocks (targeting 1GHz)
- Streamlined **AMS design workflow** by formulating a schematic-to-layout toolflow plan, improving standardization in Synopsys environments

NUST Chip Design Centre (NCDC) *Jul. 2024 – Nov. 2024*
Analog & Mixed Signal IC Design Trainee *Islamabad, Pakistan*

- Hands-on training in MOS devices, analog design cycles, schematic and layout design using **Cadence Virtuoso**
- Practical experience in designing OTAs, BGR, LDO, VCO, PLLs, and performing **DRC, LVS,** and chip sign-off processes
- Collaborated on the design of a **Passive RFID Transponder Chip** for animal tagging using **CMOS 65nm** technology

Research Experience

Pak Angels – Generative AI Training Program | GitHub *Jun. 2025 – Jul. 2025*
GenAI Trainee *Remote, Pakistan*

- Completed intensive training on **Generative AI**, ChatGPT APIs, Python, **LangChain**, **RAG systems**, and autonomous AI agents
- Delivered weekly hands-on projects and participated in final hackathon; awarded Top Performer among cohort

Information Processing & Transmission Lab, SEECS | GitHub *May 2023 – May 2024*
Research Intern *Islamabad, Pakistan*

- Designed and implemented a **Deep Deterministic Policy Gradient (DDPG)** framework integrating **Mobile Edge Computing (MEC)** and **CR-NOMA** for dynamic resource allocation in energy-harvesting IoT networks
- Published research at **IEEE WCNC 2024**, demonstrating faster convergence and superior performance over baseline offloading methods (random, always, never offloading)
- **Tech Stack:** Python, TensorFlow, Deep RL (DDPG), Simulation & Analysis

CNN Internship, SEECS | GitHub *Jun. 2023 – Aug. 2023*
Research Intern *Islamabad, Pakistan*

- Developed novel **Conv2D + LSTM** architectures for video-based regression tasks on the **UBFC dataset**
- Preprocessed video datasets and implemented data augmentation pipelines for training deep CNN models
- **Tech Stack:** Python, PyTorch, Keras, NumPy, Matplotlib

Publications

Optimizing Resource Allocation in MEC-Enabled CR-NOMA-Assisted IoT Networks: A DRL-Driven Strategy *May 2024*
IEEE Wireless Communications & Networking Conference (WCNC) 2024 | Dubai, UAE
Muhammad Taha Qaiser, Muhammad Sarmad Sohail, Minahil Shafqat, Syed Asad Ullah, Haejoon Jung, Syed Ali Hassan

- Proposed a **Deep Deterministic Policy Gradient (DDPG)** framework to optimize resource allocation in energy-harvesting IoT devices using **CR-NOMA** and **Mobile Edge Computing (MEC)**
- Achieved superior performance over baseline methods with faster convergence and minimized service delay

Key Projects

Passive RFID Transponder Chip Design *Aug. 2024 – Nov. 2024*
NUST Chip Design Centre | Cadence Virtuoso, CMOS 65nm *Islamabad, Pakistan*

- Designing RFID transponder chip for animal tagging, focusing on ultra-low power consumption, reliability, and market competitiveness

FYP: Optimizing Resource Allocation in NOMA Networks *May 2023 – May 2024*
IPT Lab, SEECS | Python, TensorFlow, DDPG *Islamabad, Pakistan*

- Developed a **Deep Deterministic Policy Gradient (DDPG)** agent to dynamically optimize time-sharing between data transmission and energy harvesting for resource-constrained IoT devices in CR-NOMA systems
- Achieved minimized service delay through extensive simulation, outperforming baseline methods with faster convergence and robust performance
- Published findings at **IEEE WCNC 2024**, demonstrating novel framework for computation offloading in MEC-enabled networks

4-bit Microprocessor and VGA Line Drawing *Apr. 2023 – Jun. 2023*
SEECS, NUST | Verilog, FPGA *Islamabad, Pakistan*

- Designed a custom 4-bit microprocessor with hierarchical datapath and control logic; implemented VGA line-drawing algorithms in **Verilog** for FPGA deployment

Radar Systems Fundamentals *Jan. 2024 – Mar. 2024*
Radar Research Lab, SINES | MATLAB *Islamabad, Pakistan*

- Studied radar system fundamentals, focusing on beamforming and signal processing techniques using MATLAB
- Gained foundational knowledge of radar concepts and their real-world applications through MIT OpenCourseWare

Skills

Programming: Python, MATLAB, C/C++, Verilog, SQL, Bash

Data & MLOps: PySpark, FastAPI, ETL Pipelines, Statistical Profiling, Feature Engineering, Synthetic Data Generation

Machine Learning: TensorFlow, PyTorch, Deep RL (DDPG), Transformers, Generative AI, RAG, LangChain

IC Design Tools: Cadence Virtuoso (ADE), Synopsys Custom Compiler (PrimeSim/PrimeWave)

Other Tools: LaTeX, Git, FPGA Design (Verilog)

Awards & Honors

NUST Merit Scholarship – Perfect 4.00 CGPA in multiple semesters *2022 & 2023*

PM's Youth Laptop Scheme (Phase III) – Government of Pakistan *2023*

Merit Scholarship – Pre-Engineering | Awarded for 2 consecutive years *2018 – 2020*